

REMARKS

This paper is being provided in response to the October 24, 2003 Office Action for the above-referenced application. In this response, Applicants have amended claims 1, 9, and 10 and added new claims 18-34 to clarify that which Applicants deem to be the invention. Applicants respectfully submit that the modifications to the claims and the new claims are all supported by the originally filed application.

The rejection of Claims 1-17 under 35 U.S.C. 102 as being anticipated by U.S. Patent No. 5,630,130 to Perotto (hereinafter "Perotto") is hereby traversed and reconsideration thereof is respectfully requested in view of amendments to the claims contained herein. Applicants respectfully submit that Claims 1-17 are patentable over Perotto for reasons set forth in detail below.

Claim 1, as amended herein, recites a method of providing one of a plurality of schedulers for a multitasking system for a processor. The method includes choosing a particular one of the schedulers, where at least one of the plurality of schedulers selects processes to be run from a plurality of runnable processes different from the plurality of schedulers, setting a program counter to an address corresponding to code of the particular one of the schedulers, and the processor executing code at an address corresponding to the program counter. Claims 2-8 depend directly or indirectly from claim 1.

Claim 9, as amended herein, recites a method of scheduling tasks in a multitasking operating system. The method includes choosing a particular one of a plurality of schedulers, where at least one of the plurality of schedulers selects processes to be run from a plurality of runnable processes different from the plurality of schedulers, and running the particular scheduler to schedule tasks. Claims 10-17 depend, directly or indirectly, from claim 9.

Perotto discloses a multitasking controller having task storage means (2) for storing up to N tasks (P0,P1,P2,P3) where each task comprises a sequence of instructions. The controller also includes a microprocessor for processing, by time-sharing, a plurality of such N tasks, and a random access memory (12) for storing variable data created and used by said microprocessor. The microprocessor further includes a scheduler (7) realized in hardware for controlling the use of the microprocessor or by such processes, and program counter storage means for storing N program counters (Pc0,Pc1,Pc2,Pc3) each for use by the scheduler (7), which is able select a different one of the program counters (Pc0,Pc1,Pc2,Pc3) when the task processed by the microprocessor is changed without the transfer of data from the random access memory (12).

Applicants respectfully submit that Perotto does not show, teach, or suggest the feature of applicants' present claimed invention of choosing a particular one of a plurality of schedulers wherein at least one of the plurality of schedulers selects processes to be run from a plurality of runnable processes different from the plurality of schedulers. Applicants' independent claims all recite more than one scheduler ("a plurality of

schedulers”) and recite that at least one of the plurality of schedulers selects processes to be run from a plurality of runnable processes different from the plurality of schedulers. In contrast, Perotto discloses a *single* scheduler that schedules one of the four disclosed tasks (P0, P1, P2, P3), none of which themselves schedule other tasks. That is, the present claimed invention recites using *a plurality of schedulers*, where at least one of the schedulers schedules tasks whereas Perotto discloses only a *single scheduler* (the hardware scheduler 7). Note that even if the single scheduler (7) of Perotto is arguably configurable, it is still distinguishable from the present claimed invention and that, in fact, the distinction is specifically made in the present application, which states on page 23, lines 4-8:

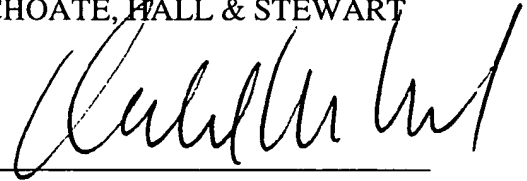
This may be distinguished from situations where a single scheduler runs one of a plurality of scheduling algorithms since, in such single scheduler/multiple algorithm situations, the scheduler may experience significant overhead in connection with determining which scheduling algorithm to run. In contrast, the multiple scheduler technique disclosed herein may avoid such overhead.

In addition to avoiding the overhead associated with techniques like those disclosed in Perotto, the present claimed invention provides additional advantages. For example, the present claimed invention allows for convenient code profiling (see discussion at page 23, beginning at line 9). Other advantages are discussed on page 23, beginning at line 23.

In view of the foregoing, Applicants respectfully submits that Perotto does not show, teach, or suggest applicants’ Claims 1-17 (or new claims 18-34) and thus applicants respectfully request that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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Date

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